What is claimed is:

1. A method for forming a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of silicon germanium having a layer of strained silicon formed thereon, and having a gate insulator formed on the strained silicon layer, a gate formed on the gate insulator, and shallow source and drain extensions formed at opposing sides of the gate;

forming a spacer around the gate and gate insulator;

etching the strained silicon layer and the silicon germanium layer to form trenches at said opposing sides of the gate;

forming silicon regions in the trenches; and

implanting deep source and drain regions in the silicon regions at said opposing sides of the gate, wherein a depth of the deep source and drain regions after said implanting does not extend beyond a depth of the silicon regions.

2. The method claimed in claim 1, further comprising annealing to activate dopants.

3. The method claimed in claim 2, wherein, after annealing, the depth of the deep source and drain regions does not extend beyond the depth of the silicon regions.

4. The method claimed in claim 2, further comprising forming silicide source and drain contacts and a silicide gate contact.

5. The method claimed in claim 4, wherein the silicide source and drain contacts and silicide gate contact comprise nickel.

6. The method claimed in claim 1, wherein the silicon germanium layer has a composition $Si_{1-x}Ge_x$, where x is in the range of .1 to .3.

7. The method claimed in claim 1, wherein the gate comprises polysilicon.

8. The method claimed in claim 1, wherein providing the substrate comprises:

patterning a gate conductive layer and a gate insulating layer to form said gate and gate insulator over said strained silicon layer.

9. The method claimed in claim 8, wherein providing the substrate further comprises:

forming a thin spacer around the gate and gate insulator; and

implanting said shallow source and drain extensions,

wherein said spacer is formed around said thin spacer.

10. The method claimed in claim 9, wherein implanting source and drain extensions is preceded by implanting halo regions at opposing sides of a channel region, the halo regions extending toward the channel region beyond ends of the source and drain extensions to be formed, the halo regions comprising a dopant having a conductivity type opposite to the conductivity type of a dopant of the source and drain extensions.

11. The method claimed in claim 1, wherein the silicon regions are formed in the trenches by selective epitaxial growth.

12. The method claimed in claim 1, wherein the substrate further comprises shallow trench isolations.

13. The method claimed in claim 1, wherein implanting the deep source and drain regions is preceded by forming a second spacer around the spacer after forming silicon regions in the trenches.

14. A method for forming a metal oxide semiconductor field effect transistor (MOSFET), comprising:

providing a substrate comprising a layer of silicon germanium having a layer of strained silicon formed thereon, a gate insulating layer formed on the strained silicon layer, and a gate conductive layer formed on the gate insulating layer;

patterning the gate conductive layer and a gate insulating layer to form said gate and gate insulator over said strained silicon layer;

forming a first spacer around the gate and gate insulator; and

implanting shallow source and drain extensions

forming a second spacer around the first spacer;

etching the strained silicon layer and the silicon germanium layer to form trenches at said opposing sides of the gate;

forming silicon regions in the trenches; and

implanting deep source and drain regions in the silicon regions at said opposing sides of the gate, wherein a depth of the deep source and drain regions after said implanting does not extend beyond a depth of the silicon regions; and

annealing to activate implanted dopants,

wherein, after annealing, the depth of the deep source and drain regions does not extend beyond the depth of the silicon regions.